**LESSON PLAN**

**Subject : DDT HDL**

**Branch: M.Tech (VLSI&DECS) Semester: I Academic Year:2016-2017**

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| **Period** | **Date (Tentative)** | **Topic** | **Unit No.** | **Teaching Methodology** | **Remarks** | **Corrective action upon review** |
|  |  | **INTRODUCTION TO HDL** | **I** |  |  |  |
| 1 | **22-08-16** | ASIC Design flow |  | Chalk & Board |  |  |
| 2 | **23-08-16** | FPGA Design flow |  | **,,** |  |  |
| 3 | **25-08-16** | comparison between ASIC Design flow and FPGA Design flow |  | **,,** |  |  |
| 4 | **26-8-16** | Features of Verilog HDL |  | **,,** |  |  |
| 5 | **29-08-16** | different Levels of Design Description, Simulation, Test bench Simulation and Synthesis process, |  | **,,** |  |  |
| 6 | **30-08-16** | Keywords, Identifiers, White Space Characters, Comments, |  | **,,** |  |  |
| 7 | **01-09-16** | Numbers, Strings, Logic Values, Strengths |  | **,,** |  |  |
| 8 | **02-09-16** | Data Types |  | **,,** |  |  |
| 9 | **05-09-16** | Data Types |  | **,,** |  |  |
| 10 | **06-09-16** | Scalars and Vectors, Parameters, Memory |  | **,,** |  |  |
| 11 | **08-09-16** | Operators, System Tasks, Exercises. |  | **,,** |  |  |
|  |  | **GATE LEVEL MODELING** | **II** | Chalk & Board |  |  |
| 12 | **09-09-16** | AND Gate Primitive |  | **,,** |  |  |
| 13 | **12-09-16** | Module Structure, Other Gate Primitives, |  | **,,** |  |  |
| 14 | **13-09-16** | Illustrative Examples, Tri-State Gates |  | **,,** |  |  |
| 15 | **15-09-16** | Array of Instances of Primitives, |  | **,,** |  |  |
| 16 | **16-09-16** | Additional Examples |  | **,,** |  |  |
| 17 | **19-09-16** | Design of Flip flops with Gate Primitives |  | **,,** |  |  |
| 18 | **20-09-16** | Delays, Strengths and Contention Resolutio |  | **,,** |  |  |
| 19 | **22-09-16** | Net Types |  | **,,** |  |  |
| 20 |  | Design of Basic Circuits |  | **,,** |  |  |
|  |  | **BEHAVIORAL MODELING** | **III** |  |  |  |
| 21 | **23-09-16** | Operations and Assignments, |  | **,,** |  |  |
| 22 | **26-09-16** | Functional Bifurcation |  | **,,** |  |  |
| 23 | **27-09-16** | Initial Construct, Always Construct, Examples |  | **,,** |  |  |
| 24 | **29-09-16** | Assignments with Delays, Wait construct |  | **,,** |  |  |
| 25 | **30-09-16** | Multiple Always Blocks, Designs at Behavioral Level |  | **,,** |  |  |
| 26 | **03-10-16** | Blocking and Non blocking Assignments |  | **,,** |  |  |
| 27 | **04-10-16** | Simulation Flow |  | **,,** |  |  |
| 28 | **06-10-16** | iƒ and iƒ-else constructs, assign-deassign construct, |  | **,,** |  |  |
| 29 | **13-10-16** | repeat construct, for loop, the disable construct, while loop |  | **,,** |  |  |
| 30 | **14-10-16** | forever loop, parallel blocks |  | **,,** |  |  |
| 31 | **17-10-16** | force-release construct, Event. |  | **,,** |  |  |
| 32 | **18-10-16** | Example programms |  | **,,** |  |  |
| 33 | **19-10-16** | Example programms |  | **,,** |  |  |
|  |  | **MODELING AT DATA &SWITCH FLOW LEVEL** | **IV** | Chalk & Board |  |  |
| 34 | **20-10-16** | , Continuous Assignment Structures, Delays and Continuous Assignments, |  | **,,** |  |  |
| 35 | **21-10-16** | Assignment to Vectors, Operators |  | **,,** |  |  |
| 36 | **01-11-16** | Verilog HDL programming for different combinational and sequential circuits |  | **,,** |  |  |
| 37 | **01-11-16** | Verilog HDL programming for different combinational and sequential circuits |  | **,,** |  |  |
| 38 | **03-11-16** | Verilog HDL programming for different combinational and sequential circuits |  | **,,** |  |  |
| 39 | **04-11-16** | Strength Contention with Trireg Nets, Exercises |  | **,,** |  |  |
| 40 | **07-11-16** | Basic Transistor Switches, CMOS Switch, Bi-directional Gates, |  | **,,** |  |  |
| 41 | **08-11-16** | Time Delays with Switch Primitives |  | **,,** |  |  |
| 42 | **10-11-16** | Instantiations with Strengths and Delays |  | **,,** |  |  |
|  |  | **SYSTEM TASKS, FUNCTIONS, AND COMPILER DIRECTIVES** | **V** | Chalk & Board |  |  |
|  |  |  |  |  |  |  |
| 43 | **14-11-16** | Parameters, Path Delays, Module Parameters |  | **,,** |  |  |
| 44 | **15-11-16** | System Tasks and Functions |  | **,,** |  |  |
| 45 | **17-11-16** | Module Parameters |  | **,,** |  |  |
| 46 | **18-11-16** | File-Based Tasks and Functions |  | **,,** |  |  |
| 47 | **21-11-16** | Compiler Directives, Hierarchical Access, General Observations, Exercises |  | **,,** |  |  |
| 48 | **22-11-16** | Function, Tasks, User- Defined Primitives (UDP), FSM Design (Moore and Mealy Machines) |  | **,,** |  |  |
|  |  | **DESIGN AND SYNTHESIS OF DATA PATH CONTROLLER** | **VI** |  |  |  |
| 49 | **24-11-16** | Partitioned Sequential Machines |  | **,,** |  |  |
| 50 | **05-12-16** | Design and Synthesis of a RISC Stored |  | **,,** |  |  |
| 51 | **06-12-16** | Program Machine |  | **,,** |  |  |
| 52 | **08-12-16** | Design example –UART |  | **,,** |  |  |
| 53 | **13-12-16** | UART Transmitter- |  | **,,** |  |  |
| 54 | **15-12-16** | UART Receiver |  |  |  |  |
| 55 | **16-12-16** | Example programms |  |  |  |  |

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